## ABSTRACT OF THE DISCLOSURE

A data latch circuit and method for improving operating speed therein may provide a reduction in delay time. The data latch circuit includes a sense amplifying unit outputting a first signal in response to input data, a first inverted signal in response to a clock signal, a second signal in response to given cascode data, and a second inverted signal in response to the clock signal. A clock latch unit may generate a gated clock signal to enable output of the given cascade data to the sense amplifying unit, in response to an enabling signal and the clock signal. A MUX unit outputs the first signal as output data and the first inverted signal as feedback data, or outputs the second signal as output data and second inverted signal as feedback data, based on the logic level of the enabling signal.